AMENDMENTS TO THE CLAIMS

Claims 1-11 (Withdrawn)

Claim 12 (Currently Amended) An asymmetric field effect transistor (FET) comprising:

a patterned stack including at least a vertical semiconductor body having exposed sidewalls located on an upper surface of a substrate;

a gate dielectric located on each exposed sidewall of said vertical semiconductor body;

a p-type gate portion located on one side of the vertical semiconductor body and an n-type portion located on an opposing side of the ~~on a~~ vertical semiconductor body, said gate portions are located on said upper surface of the substrate and are separated from the vertical semiconductor body by said gate dielectric;

an interconnect ~~between~~ located at least over said p-type gate portion and said n-type gate portion; and

a planarizing structure above said interconnect.

13. (Currently Amended) The asymmetric FET of Claim 12 wherein said p-type gate portion, said n-type gate portion, said interconnect, and said planarizing structure have ~~a lateral dimension that are~~ substantially the same final shape.

14. (Original) The asymmetric FET of Claim 12 wherein said p-type gate portion, said n-type gate portion and said planarizing structure are composed of a polySi-containing material or a semiconducting material.

15. (Original) The asymmetric FET structure of Claim 14 wherein said polySi-containing material comprises polySi or polySiGe.

16. (Original) The asymmetric FET of Claim 12 wherein said interconnect is highly resistant to dopant diffusion.

17. (Original) The asymmetric FET of Claim 12 wherein said interconnect is a conductive metal, metal silicide or metal nitride.

18. (Original) The asymmetric FET of Claim 12 wherein said planarizing structure is doped polysilicon.

19. (Cancelled)

20. (Original) The asymmetric FET of Claim 12 wherein said vertical semiconductor body has a hard mask present on an upper surface.

21. (Original) The asymmetric FET of Claim 20 wherein said hard mask is comprised of an oxide, nitride, oynitride or multilayers thereof.

22. (Original) The asymmetric FET of Claim 12 wherein said n-type gate portion is comprised of N-doped polysilicon and said p-type gate portion is comprised of P-type polysilicon.

23. (Currently Amended) The asymmetric FET of Claim 12 wherein ~~said vertical semiconductor body is formed atop a substrate,~~ said substrate comprises an upper insulating portion and a lower semiconducting portion.

24. (Original) The asymmetric FET of Claim 23 wherein said vertical semiconductor body and said substrate are components of a silicon-on-insulator material.

25. (Original) The asymmetric FET of Claim 12 wherein said planarizing material is a metal or metal alloy.

26. (Original) The asymmetric FET of Claim 12 further comprising source/drain regions in areas adjacent to the vertical semiconductor body.

27. (Original) The asymmetric FET of Claim 26 wherein said source/drain regions are doped so as to have either donor or acceptor impurities.

28. (Currently Amended) An asymmetric field effect transistor (FET) comprising:

a patterned stack including at least a vertical single crystal Si semiconductor body having exposed sidewalls located on an upper surface of a substrate;

a gate dielectric located on each exposed sidewall of said vertical single crystal Si semiconductor body;

a p-type gate portion located on one side of the vertical single crystal Si semiconductor body and an n-type gate portion located on an opposing side of the ~~on a~~ vertical single crystal Si semiconductor body, said p-type and n-type gate portions are composed of polysilicon, and said gate portions are located on said upper surface of the substrate and are separated from the vertical single crystal Si semiconductor body by said gate dielectric;

a metal silicide interconnect ~~between~~ located at least over said p-type gate portion and said n-type gate portion; and

a planarizing doped polysilicon layer above said interconnect.